ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

A Bridgeless High Power Factor Buck Converter Based Dual Output SMPS

Vidhya N Elayath[1], Chitra Sabu[2]

PG Student [PE], Dept. of EEE, Sree Narayana Gurukulam College of Engineering, Kadayiruppu, Kerala, India[1]

Assistant Professor, Dept. of EEE, Sree Narayana Gurukulam College of Engineering, Kadayiruppu, Kerala, India[2]

ABSTRACT: This paper introduces a bridgeless high power factor buck converter based dual output SMPS particularly for low power applications. The recently modified improved power quality SMPS topologies are designed for medium and high power applications. When they are used for low power applications their efficiency will be very low. The proposed SMPS specially designed for low power applications. It consisting of a bridgeless buck converter front end designed to operate in discontinuous capacitor voltage mode (DCVM), a half bridge inverter circuit, a multi winding transformer for energy transferring and isolation, and rectifier circuit at the transformer secondary. The converter has only one switch which is controlled using a voltage follower approach. As multiple outputs at low power levels are obtained it can be used for low power applications with a high efficiency and improved power factor.

KEYWORDS: Bridgeless Buck Converter, SMPS, DCVM operation, PI Controller, Half Bridge Inverter

I.INTRODUCTION

Switched Mode Power Supplies are widely used for powering up different parts in a personal computer by generating multiple Dc voltages from single phase AC supply. But SMPS operation usually suffers from low power factor at the input AC mains. The reason is the commonly used diode bridge rectifier front end of the SMPS. Bridgeless power factor correction converter at the front end of the SMPS is expected to draw a sinusoidal input current at high power factor. Improvement in power quality also results in better efficiency. The existing topologies are mainly for medium and high power applications. SEPIC and Cuk based front end topologies results in increased number of components.

This paper deals with the development of bridgeless rectifier based dual output SMPS specially designed for low power applications. It uses a bridgeless buck converter front end followed by a half bridge inverter connected to the primary side of a transformer with two secondary windings. Secondary side consisting of a rectifier - filter arrangement. The bridgeless buck converter is designed to operate in Discontinuous Capacitor Voltage Mode (DCVM), which reduces the complexity in control as well as the input filter requirements.

II.LITERATURE SURVEY

From the comprehensive study of different PFC topologies and their performance evaluations [1] it is found that, single switch converter topologies with current multiplier control in CCM operation leads to better stability. The push-pull and half-bridge (two-switch) converters have equal switching losses as compared to single switch converters such as flyback, Cuk SEPIC, and Zeta. But the control scheme seems to be more complex one.

A unity power factor multiple isolated outputs switching mode power supply using a single switch offers an improved power factor [2]. The topology is based on a SEPIC converter operating in continuous conduction mode. The SEPIC topology itself increases the number of components also CCM operation requires a complex control.

Bridgeless cuk rectifiers can also used for PFC applications [3]. It avoids the bridge circuit and uses only two semiconductor switches. The cuk topology is designed to work in discontinuous conduction mode (DCM) to achieve almost unity power factor.
Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses can be achieved using a single bidirectional switch and two fast diodes [4]. It is especially suited for high voltage and high power applications. Even

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

though it is bridgeless in nature and simple in control it requires an additional gate drive transformer. Also the SEPIC converter has the disadvantage of discontinuous output current resulting in a relatively high output ripple.

Bridgeless buck converters operating with high power factor will improves the efficiency at low line voltage [5]. The converter operates in both discontinuous current mode and continuous current mode. It reduces the conduction loss by reducing the number of simultaneously conducting components. Due to the discontinuous current mode operation it needs a large input filter circuit. Also the power factor will not be improved as much due to the CCM operation mode. Buck converter operation in DCVM reduces the input filter requirements and results in simple control circuit [6].

III.CIRCUIT DESCRIPTION

The proposed topology integrates a bridgeless buck converter operating in discontinuous capacitor voltage mode with a dual output switched mode power supply in order to improve the power quality at lower power levels. Fig. 1 shows the basic circuit diagram of the proposed topology.

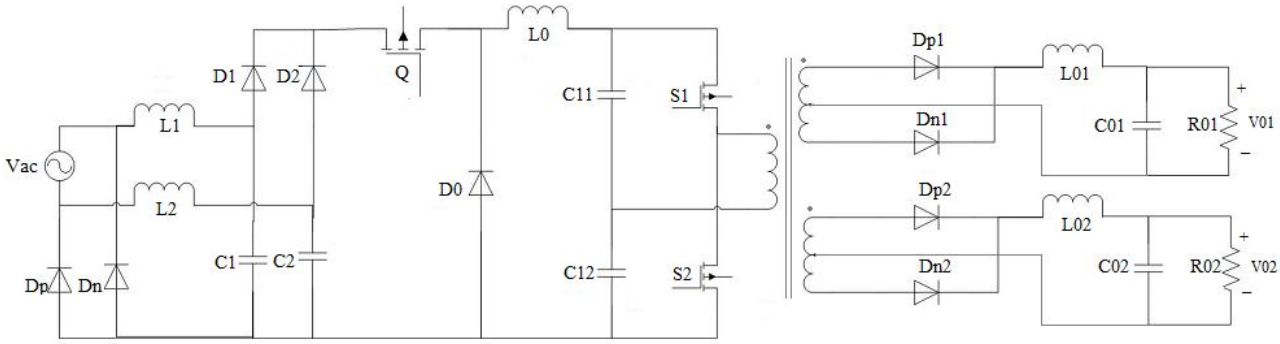

Fig. 1 Proposed circuit

Ac input is given to a buck converter which is bridgeless in nature. The bridgeless topology consists of two input inductors hence input filtering circuit can be avoided. L_1 and L_2 are supposed to be large enough to have a constant input current through them. The converter circuit consist of only a single power switch which is single quadrant in nature. Hence the switch is connected in series with two diodes D_p and D_n which are expected to conduct during positive and negative half cycles respectively. The switch can be controlled by using a DC link voltage follower approach. Care should be taken while selecting the capacitors C_1 and C_2 so that they should be operate in discontinuous operating mode. The constant DC voltage is inverted using a half bridge inverter and fed to the primary of the transformer. At the secondary side, there is a multiple diode rectifier followed by a filter circuit, which makes a pure DC output.

IV.PRINCIPLE OF OPERATION

Bridgeless Buck converter: The circuit operation of the bridgeless buck converter can be divided into three distinct topological stages. The analysis assumes the converter operates at a steady-state condition in addition to the following assumptions.

- The input is purely sinusoidal.
- L_1 and L_2 are large enough such that the current through them can be assumed constant over a switching cycle.
- C_0 is large enough so that converter output voltage is assumed to be constant.
- C_1 and C_2 should not be too large to ensure DCVM operation.

During the positive half cycle, L_1-C_1-D_1-Q-L_o-D_o is active through diode D_p, which connects the input ac source to the output ground. During the negative half-line cycle, L_2-C_2-D_2-Q-L_o-D_o is active through diode D_n, which connects the input ac source to the output ground.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

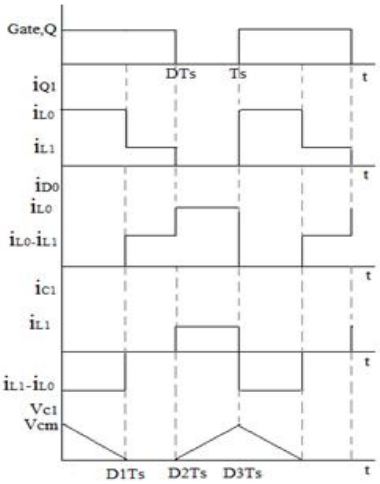

Fig. 2 Switching Waveforms

Mode 1($0 \leq t \leq D_1T_s$): In this mode converter switch Q is turned on. Input capacitor c_1 is discharging from its maximum voltage V_{cm}. Output inductor current will be equal to the switch current. Voltage across the capacitor C_1 keeps the freewheeling diode reverse biased. This mode ends when the capacitor discharges completely.

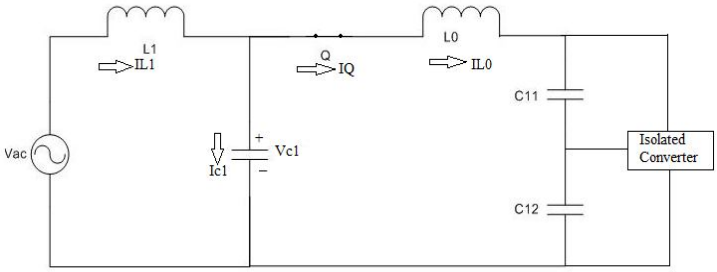

Fig. 3 Converter Mode 1 Operation

Mode 2 ($D_1T_s \leq t \leq DT_s$): Switch Q is still conducting. The switch current will be equal to the input inductor current. Capacitor C_1 stays completely discharged. Freewheeling diode become forward biased and starts conducting. This stage ends by the removal of switch gating pulse.

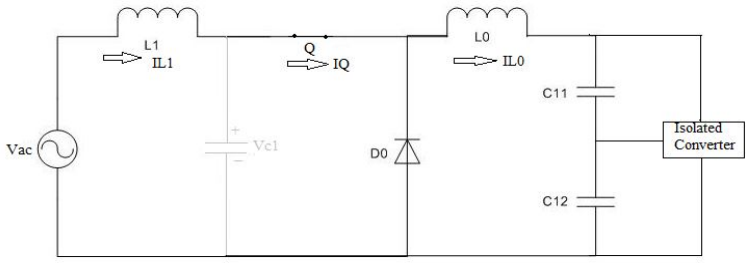

Fig. 4 Converter Mode 2 Operation

Mode 3 ($DT_s \leq t \leq T_s$): During this interval switch Q is off. Input capacitor C_1 starts charging through the input Inductor from zero to its maximum voltage V_{cm}. Freewheeling diode is still conducting.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

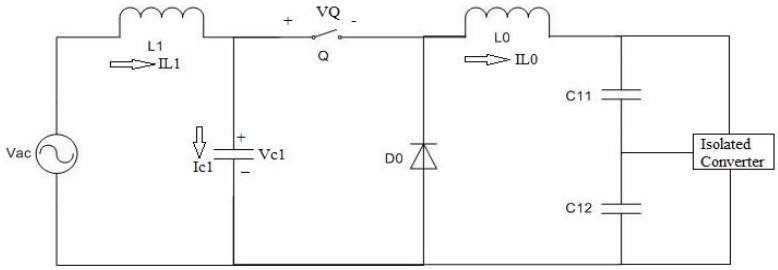

Fig. 5 Converter Mode 3 Operation

Half Bridge Inverter: The regulated DC output voltage of the bridgeless buck PFC converter is fed to the half bridge voltage source inverter circuit for scaling and isolation purpose. The circuit operation of the half bridge inverter over one switching cycle is divided into four stages.

Mode 1: In the first mode, the upper switch S_1 is turned on; the input current circulates through the primary winding of the HFT to the lower input capacitor C_{12}. Upper diodes at the secondary side start conducting. Output inductors L_{01} and L_{02} will charge through the upper diodes.

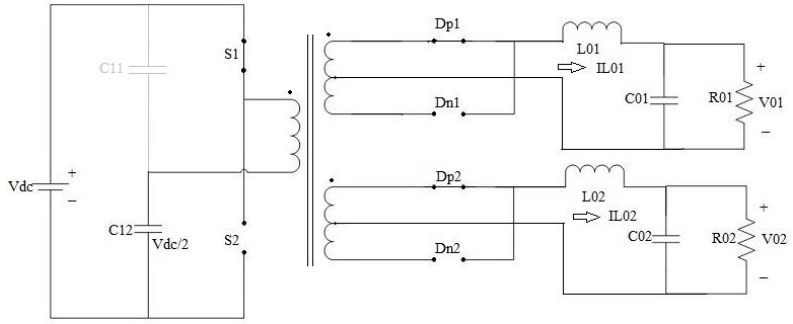

Fig. 6 Half bridge VSI Mode 1- When switch S_1 on

Mode 2: During this interval both the switches are in off state. All the diodes will be freewheeling since the inductors discharges through the diodes.

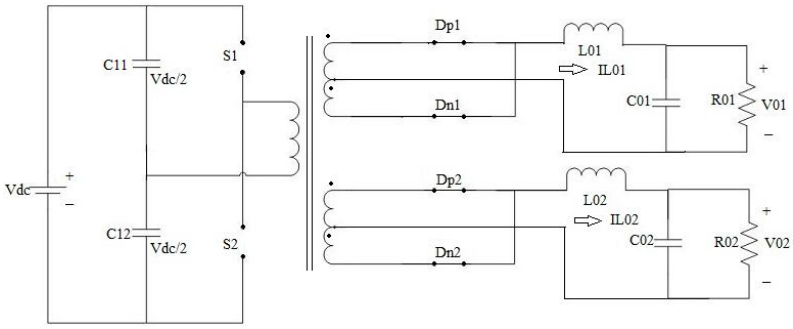

Fig. 7 Half bridge VSI Mode 2 – when both switches are off

Mode 3: In this mode S_2 is turned on, and the input current flows through upper capacitor C_{11} and the primary winding. Lower diodes in the secondary windings forward biased, and output inductors start storing energy.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

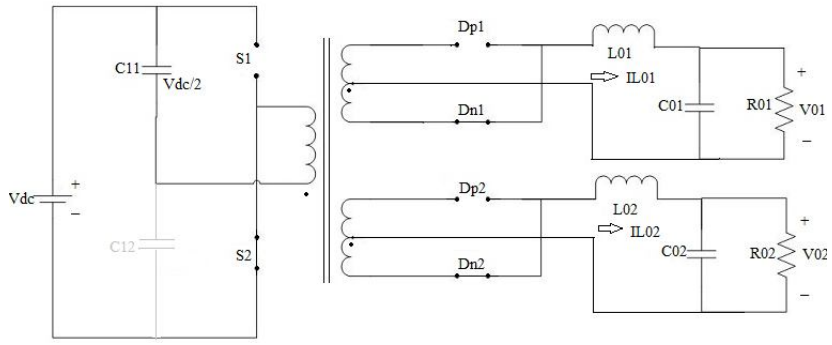

Fig. 8 Half bridge VSI Mode 3 – when switch S_2 is on

Mode 4: Mode for is same as mode 2, where both the switches at the primary side are off and all the secondary diodes freewheeling.

V. SIMULINK MODEL

To verify the feasibility and validity of the proposed converter, MATLAB/ Simulink software is applied for the simulation of the SMPS at an operating point of input voltage V_{ac} = 100 V_{rms} @ 50 Hz and f_s = 50 kHz. Performance of the proposed multiple-output SMPS is simulated in MATLAB/Simulink environment using Sim-Power- System toolbox and discrete time sampling. The duty cycle is set to 48.3%. Fig. 9 shows the Simulink model of the proposed SMPS. The following parameters are used for simulation modeling. L_1= L_2= 2.2mH, L_0 = 180 µH, C_1= C_2= 47nF, C_{11}=C_{12}= 3000 µF, C_{01}=C_{02}=330nF, L_{01}=L_{02}=3.5 mH.

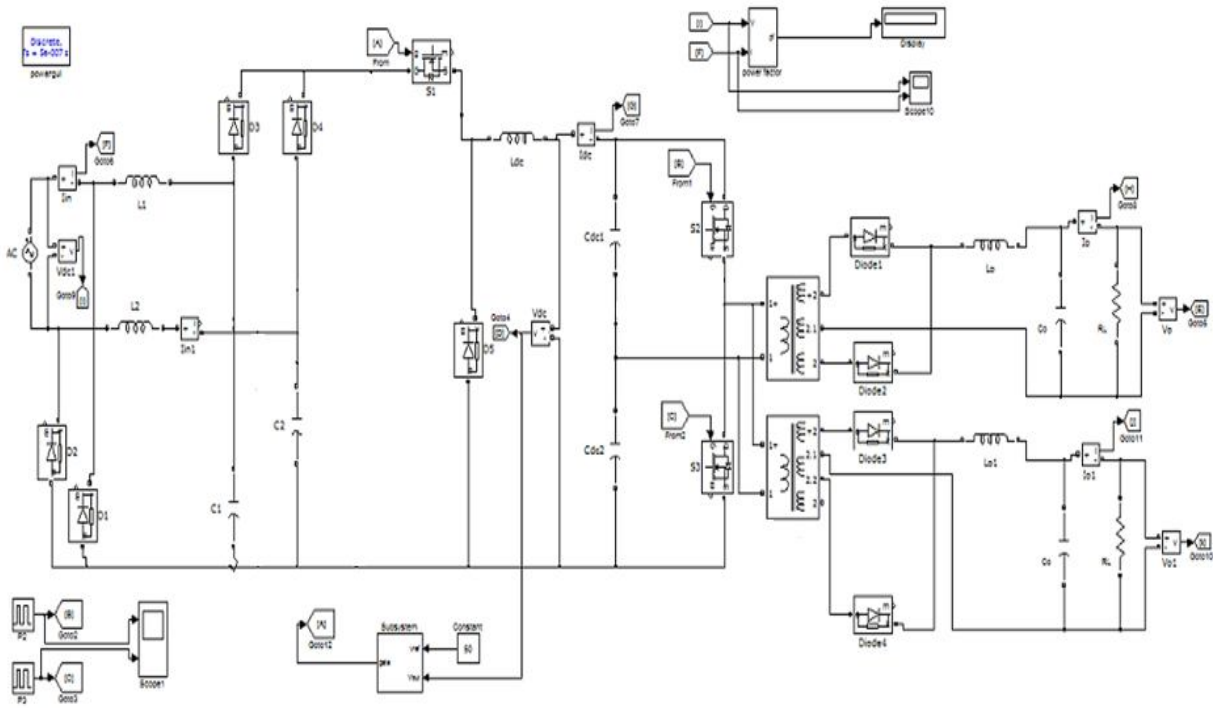

Fig. 9 Simulink Model

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

VI. REUSLT AND DISCUSSION

Fig. 10 shows the input voltage waveform. Input voltage is 100 v_{rms} at 50 Hz.

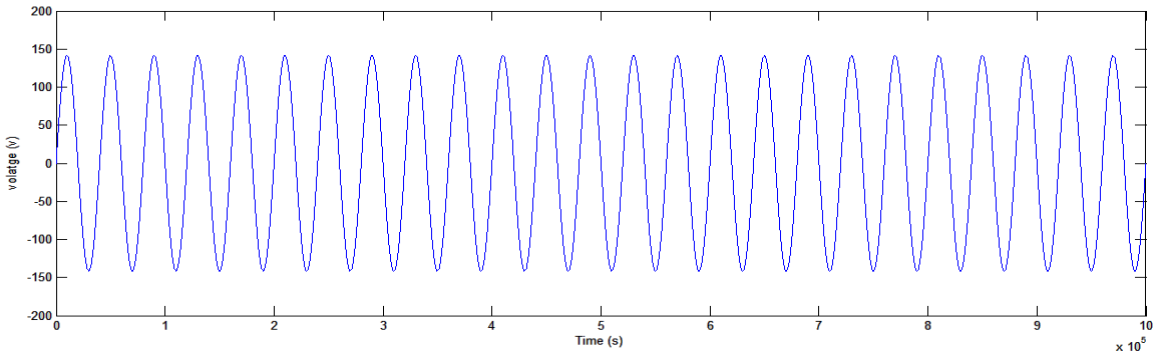

Fig .10 Input Voltage

Fig. 11 shows input current waveform. It is clear from the figure that the input current is sinusoidal and is in phase with the ac input voltage, at a power factor of 0.999.

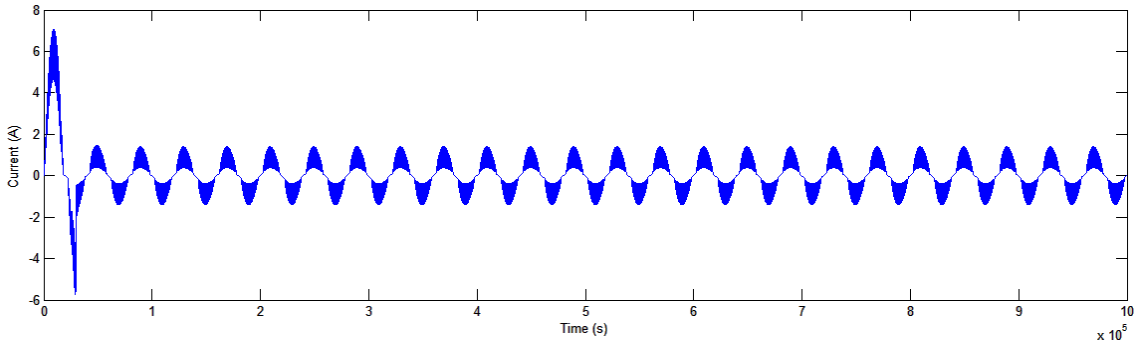

Fig .11 Input Current

Enlarged view of capacitor voltages under positive and negative half cycles is shown. The input capacitors are operating in the discontinuous capacitor voltage mode.

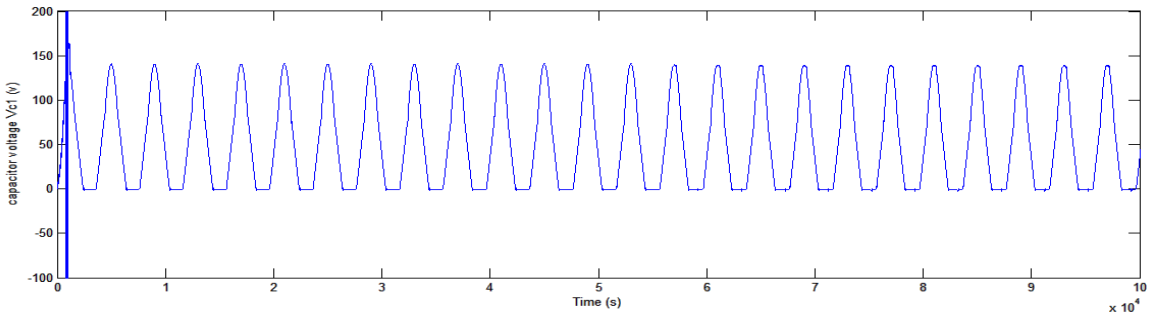

Fig. 12 Input capacitor voltage V_{c1}

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

The capacitor C_1 operates during positive half cycle and C_2 operate in the negative half cycles of the input voltage.

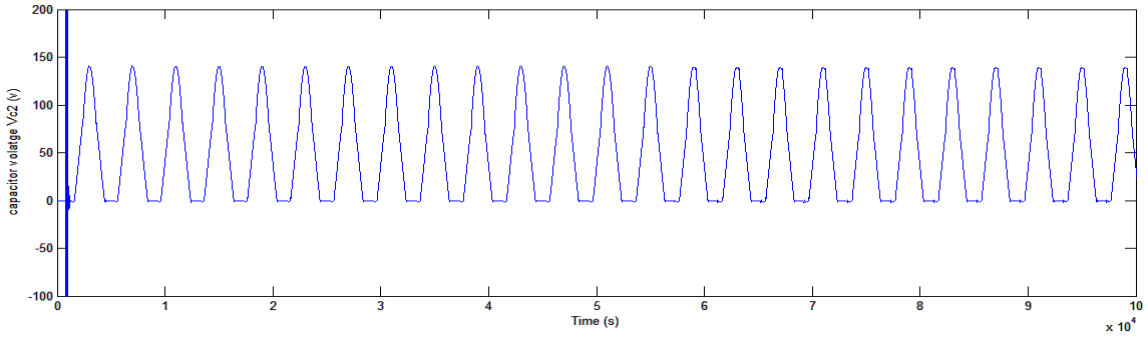

Fig. 13 Input capacitor voltage V_{c2}

Fig. 14 shows SMPS output voltage waveforms V_{01} at 9V. Due to the constant DC link voltage control it is possible to obtain a constant DC voltage at the output with minimum ripples.

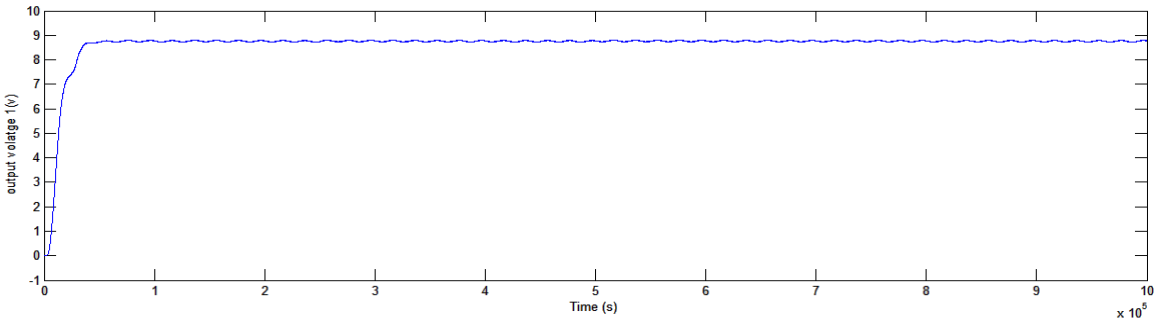

Fig. 14 SMPS output voltage waveform V_{01}

Fig. 15 shows SMPS output voltage waveforms V_{02} at 6V. Steady state value is achieved within 3 switching cycles.

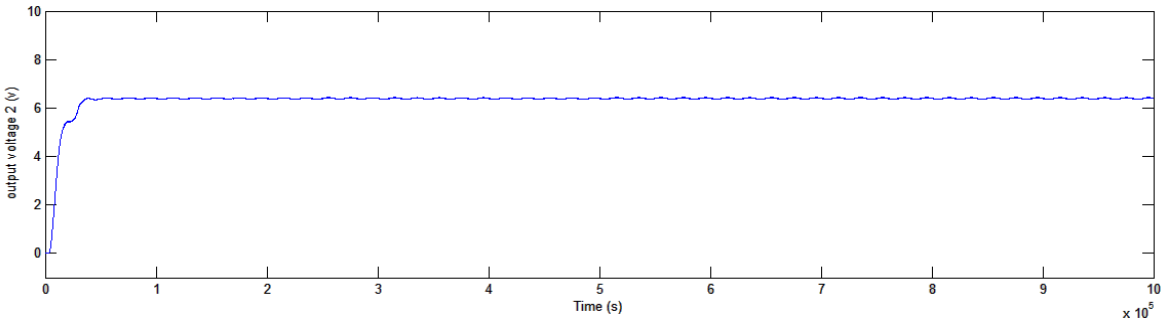

Fig. 15 SMPS output voltage waveform V_{02}

Fig. 16 shows the SMPS output current waveform $I_{01,}$ which is 0.6 A. It is clear that the output current is constant.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 4, Issue 9, September 2015

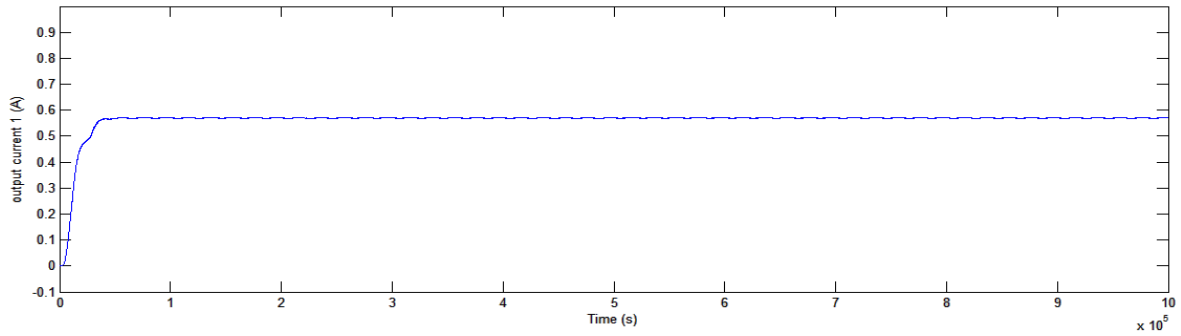

Fig. 16 SMPS output current waveform I_{01}

Fig. 17 shows the SMPS output current waveform $I_{02,}$ which is 0.4 A. Steady state value is achieved within 3 switching cycles.

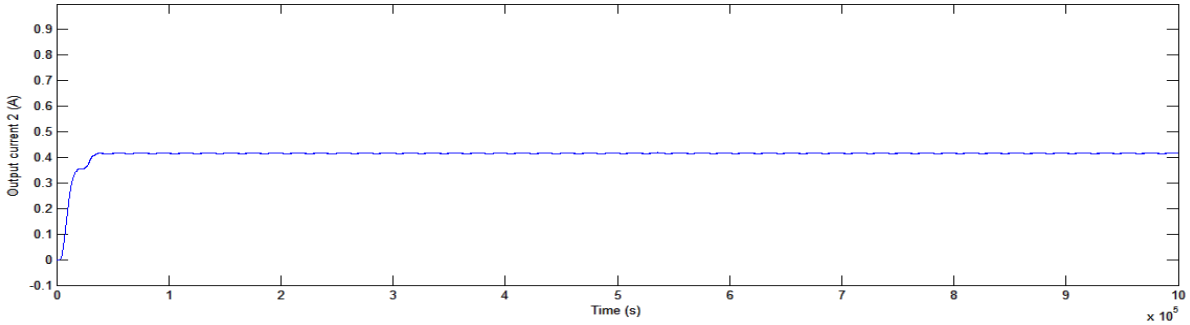

Fig. 17 SMPS output current waveform I_{02}

VI.CONCLUSION

A high power factor bridgeless buck converter based dual output SMPS has been designed for low power applications. The main advantages of the proposed system include improved power factor operation, reduced component count, cost reduction and simple control. By the careful selection of input capacitors it is possible to obtain DCVM operation of the front end converter. The operation of circuit is analyzed, and simulated the performance characteristics. From the simulation results it is found that for a 100 V input the front end converter produces a 48 V output voltage with 96 % conversion efficiency. Also DCVM operation of the input capacitors is achieved. Dual output SMPS with input power factor 0.999 is successfully obtained at output voltages of 9V and 6V respectively.

REFERENCES

[1] B. Singh *et al.*, "A review of single-phase improved power quality AC–Dc converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003

[2] A. Canesin and I. Barbi, "A unity power factor multiple isolated outputs switching mode power supply using a single switch," in *Proc. IEEE APEC*, Mar. 1991, pp. 430–436

[3] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "New efficient bridgeless Cuk rectifiers for PFC applications," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3292–3301, Jul. 2012

[4] E. H. Ismail, "Bridgeless SEPIC rectifier with unity power factor and reduced conduction losses," *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Apr. 2009

[5] Y. Jang and M. M. Jovanovi´c, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011

[6] Abbas A. Fardoun et al., "Bridgeless High-Power-Factor Buck-Converter Operating in Discontinuous Capacitor Voltage Mode," *IEEE Trans. Ind. Appln.*, vol. 50, no. 5, pp. 3457–67, Sept. 2014.